Dynamic Synchronizer Flip-Flop Performance in FinFET Technologies

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***Abstract*—The use of fine-grain Dynamic Voltage and Frequency Scaling (DVFS) has increased the number of distinct clock domains on a given Network-on-Chip (NoC). This necessitates robust synchronizers to prevent clock domain communication failures, even as FinFET devices have begun to replace planar devices. This paper presents simulation results and comparisons between dynamic (requiring reset) and non-dynamic synchronizer flip-flops implemented in predictive models for both planar technologies and future FinFET technologies. Results demonstrate that synchronizers built with FinFET devices 1) exhibit a tau value which continues to scale with fan-out of four delay and 2) can be improved with forward biasing, but 3) are more sensitive to temperature. Dynamic flip-flops settled metastability fastest when using standard technology voltages, but previously couldn't be used in non-dynamic systems. For this reason, a new synchronizer design is also presented which exploits the benefits of dynamic flip-flops without the need for a dedicated reset signal.**

***Keywords*—NoC, GALS, Synchronizers, Metastability, FinFET**

I. Introduction

Both the increase in the number of independent cores per system, and the use of fine grained Dynamic Voltage and Frequency Scaling (DVFS), has led to an increase in the number of clock domains per Network-on-Chip (NoC). Communication across these clock domains often requires the use of "brute force" synchronizers which rely on highly optimized synchronizer flip-flops connected in series. As CMOS continues to scale, circuit designers must re-evaluate design trade-offs for each new technology node. Now that semiconductor manufacturers are moving from planar CMOS to FinFET CMOS, circuit designers must prepare for changes of an even larger scale.

Previous work has focused on the effect of technology scaling on synchronizers in planar technology [1]–[5], but this paper aims to demonstrate the effects of FinFET devices. To evaluate their effects, HSPICE simulations using predictive technology models developed at ASU [6] were performed and compared with theoretical analysis. While on-chip synchronizer evaluation techniques have been developed [7], building test chips for multiple technology nodes would be both prohibitively expensive and impossible for nodes not yet in production (such as 10nm and 7nm). This paper's key contributions include simulation results and theoretical analysis on three high performance synchronizer flip-flops in five different technology nodes. The simulation results presented in this paper demonstrate the continual relationship between tau (τ) and fan-out of four ($FO4$) delay even in FinFET devices. It was also found that body biasing synchronizer feedback loops is still effective in FinFET devices, but not as significant as with planar devices. FinFET synchronizers were also observed to be more sensitive to temperature variations. The Dynamic Latch Flip-Flop performed the best at standard voltage levels. For this reason, this paper also presents The Dynamic Synchronizer, which enables the use of dynamic synchronizing flip-flops in non-dynamic systems.

II. Background

When communicating across clock domains the transmitted data and receiving clock are not aligned. Therefore setup and hold times are likely to be violated, possibly causing metastability. Metastability occurs when the bi-stable element within the flip-flop does not have enough time to fully charge or discharge, resulting in a half-charged element. This half-charge is usually very close to ($\frac{V_{DD}}{2}$), and is not logic high or logic low. The element will eventually settle, but it is impossible to predict when the settling will occur or which state it will settle to. Brute force synchronizers are designed as a chain of flip-flops connected in series, and reduce the possibility of metastability entering the receive domain's logic. Each additional flip-flop reduces the possibility of metastability, but the synchronizer will always retain a finite chance of failure (metastability manifesting on the output). Since additional flip-flops also result in an increased latency through the synchronizer, a trade-off between latency and reliability exists. To quantify the frequency of these failures, brute force synchronizer reliability is commonly expressed as the Mean Time Between Failures (MTBF). The expression in Equation (1) shows dependence on the receiver clock frequency (F_C) and incoming data frequency (F_D). These factors are independent of the flip-flops within the synchronizer, and so these factors are assumed to not change with technology scaling. The factor S is defined as the settling time, and is often simplified as the receiver clock period multiplied by the number of flip-flop stages. This is generally a design parameter which can be varied to achieve the desired MTBF. Since this factor is not dependent on the properties of the individual flip-flops, it is unaffected by process technology.

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W F_C F_D} \tag{1}$$

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T_W (the sensitive region) and τ (evaluation time constant) are both dependent on the individual flip-flop however, and are therefore affected by changes in process technology. Although some papers have considered the effects of T_W [7], T_W only affects MTBF linearly while τ is exponential. For this reason, much of the past work has chosen to focus on τ rather than T_W [8], [9]. More complex expressions have been proposed for accurately calculating the MTBF of multi-stage synchronizers; but these expressions still show that τ is the most dominant factor [10].

The value of τ can be affected by many environmental factors, but circuit structure plays a central role. Two circuit parameters of particular importance are transistor strength and node capacitance. A number of circuit topologies have been designed to minimize the necessary node capacitance, while also improving the gain of the flip-flop feedback loop [2], [9], [11]–[14]. Device sizing is also important, and so a multitude of techniques have been proposed to effectively manage the tradeoff between device strength and size [2], [13], [15]. Some techniques have also considered adding supplementary devices but these studies have had mixed results [14], [16].

Naturally, both transistor strength and node capacitance change as technology scales. One key parameter used to compare technology nodes is the fan out of four delay (commonly referred to as $FO4$). Since the early days of CMOS, designers have tracked both $FO4$ and τ, finding them to scale together [1]. As planar technology has continue to scale, some researchers claim that this trend has continued [2], [3] while others claim that after 65nm this is no longer the case [4], [5]. In this paper we demonstrate through theoretical analysis and simulation results that $FO4$ and τ, do continue to scale together both in planar and in FinFET technology.

FinFET devices offer a number of significant benefits in addition to allowing the continuation of Moore's Law. Two of the most well-known benefits of FinFET technology are decreased leakage current and less variation in Vt between process corners [17], [18]. All circuits will benefit from a decrease in leakage current, including synchronizers. Leakage is not a dominant effect on synchronizer performance however, and so this particular improvement is not considered in this work. The effect of tighter process corners will also have an impact of synchronizers since they must be designed for the worst case. The end result of this is expected to be an overall improvement in synchronizer performance, but would not affect design trade-offs. Process corners are also heavily defined by laboratory experimentation, and therefore future technology simulation models do not consider them [6].

III. Experimental Methodology

A. Simulating τ

The HSPICE simulation strategy used to generate the results found in this paper was modeled on a hardware testing methodology developed by Dike and Burton [9]. A similar simulation based adaption of this technique has recently been used in other synchronizer design research [8]. In the original hardware technique, memory cell nodes are first forced into metastable levels. For simulation, this is accomplished with initial conditions. Once forced into metastability, measurements are taken as the circuit begins to self-correct back to a stable value (a logical high or low value). The speed at which the circuit can self-correct is recorded, and used to calculate the value of τ. This gives an accurate value without needing to rely on simulation methods which require data vs. clock time sweeps. Data vs. clock time sweep τ simulation methods have proven to be unreasonable given HSPICE's sensitivity [9].

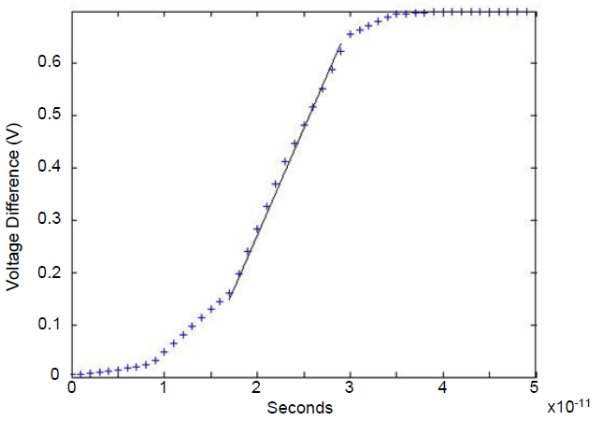


Fig. 1: Synchronizer Bi-stable Element Circuit Response

Bi-stable devices within synchronizer flip-flops generally have two sides. This is most easily understood when considering an inverter loop. When stable, the voltage of one side of the loop is at V_{DD} while the other is GND. When both sides are forced to be $\frac{V_{DD}}{2}$, the voltage difference between the two nodes is zero. As the bi-stable element begins to settle, this voltage difference begins to increase or decrease depending on the polarity. Fig.1 shows how this occurs in simulation. The properties of this change are used to calculate τ, as shown in equation (2). Two points which represent the linear section in Fig. 1 are selected, and these two points are entered into the formula as (t_1,V_1) and (t_2,V_2).

$$\tau = \frac{t_1 - t_2}{ln(V_2/V_1)} \tag{2}$$

B. Flip-flop Initialization

As described, the first step in simulation is forcing the flip-flop under test into metastability. This paper considers three synchronizer flip-flops which each utilize different bi-stable element structures. Each bi-stable element structure requires a different method of initialization.

The first flip-flop considered was the Dynamic Latch Flip-Flop (DLFF), sometimes referred to as a jamb latch flip-flop [9]. The DLFF is so named due to the dynamic nature of its circuit, which requires a separate $reset$ signal before the device can be re-evaluated (refer to Fig. 3). This modification reduces the capacitance on the element, which enables the circuit to outperform standard synchronizer flip-flops. Unfortunately it also limits the usabililty of the circuit in modern devices which very rarely contain a dynamic reset signal. Since the DLFF utilizes a simple cross-coupled inverter pair, initializing the circuit into metastability is similar to what has been just described.

The second circuit simulated was the PowerPC flip-flop, recently considered as a suitable sub-threshold voltage synchronizer flip-flop [11]. The PowerPC flip-flop as shown in Fig.4, was initialized by setting the pass gate transistor switch and all $Wp2$ and $Wn2$ devices in the ON state. The data input is then set to $\frac{V_{DD}}{2}$. The voltage difference is then considered between node X and output of the inverter consisting of $Wp1$ and $Wn1$.

The Pseudo-NMOS flip-flop is the third to be simulated, and is shown in Fig.5. This flip-flop was initially proposed as a bi-stable element which did not sharply degrade in speed as V_{DD} was reduced. To initialize the Pseudo-NMOS flip-flop, the q and $\overline{q}$ nodes were set at $\frac{V_{DD}}{2}$, and then the clock was set to low such that that mm and $\overline{mm}$ were in the same state. The voltage difference was taken between q and $\overline{q}$.

IV. Results

A. τ and $FO4$ delay

The link between synchronizer flip-flop τ values and $FO4$ delay has been used in the past to predict synchronizer τ in new technologies. Both factors rely on the device size/strength tradeoff defined by the technology node. However, the research community has disagreed about whether or not this trend continues [1]–[5]. Ginosar et al. have proposed that after 65nm, each technology node will see higher τ while $FO4$ delay will continue to decrease [4]. They justify this claim by first creating a mathematical relationship between $FO4$ delay and τ in (3).

$$\tau = \frac{\eta}{4}\frac{t_{d,FO4}}{A} \tag{3}$$

Equation 3 represents τ as a function of $FO4$ delay, A (inverter gain), and η (derived from a combination of V_{DD}, V_t, and λ). It was proposed that while $FO4$ will continue to scale, the inverter gain will not, creating a degradation in τ [4]. Other researchers have released results demonstrating τ values which continue to track $FO4$ delay [2]. Until now, the

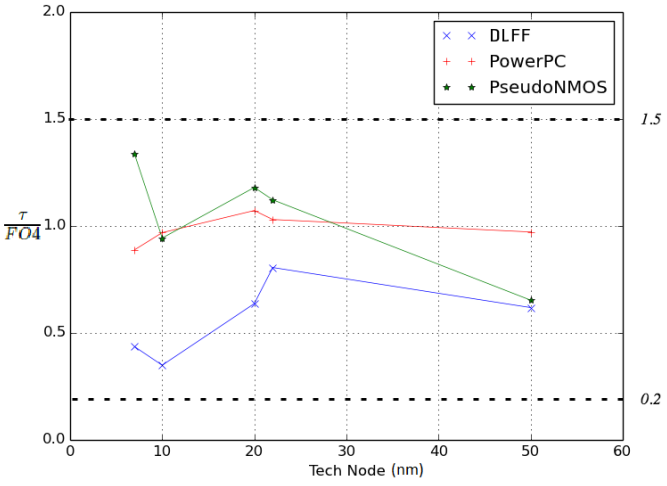


Fig. 2: $\frac{\tau}{FO4}$ For Planar and FinFET Nodes

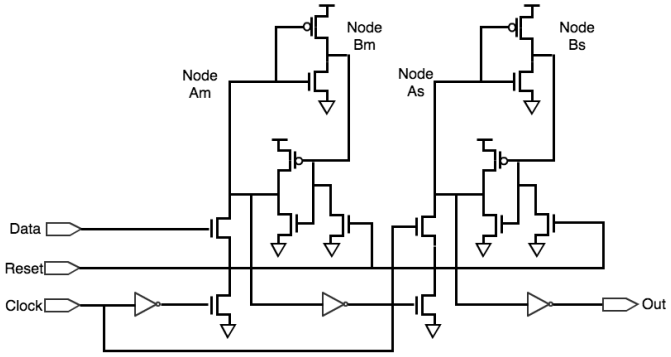


Fig. 3: Dynamic Latch Flip-Flop [9]

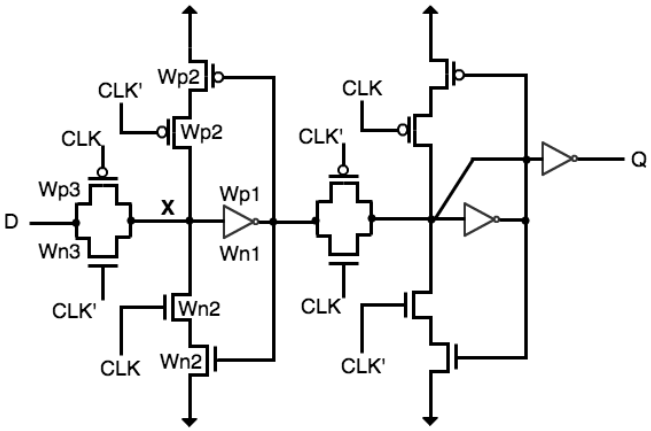


Fig. 4: PowerPC Flip-Flop [11]

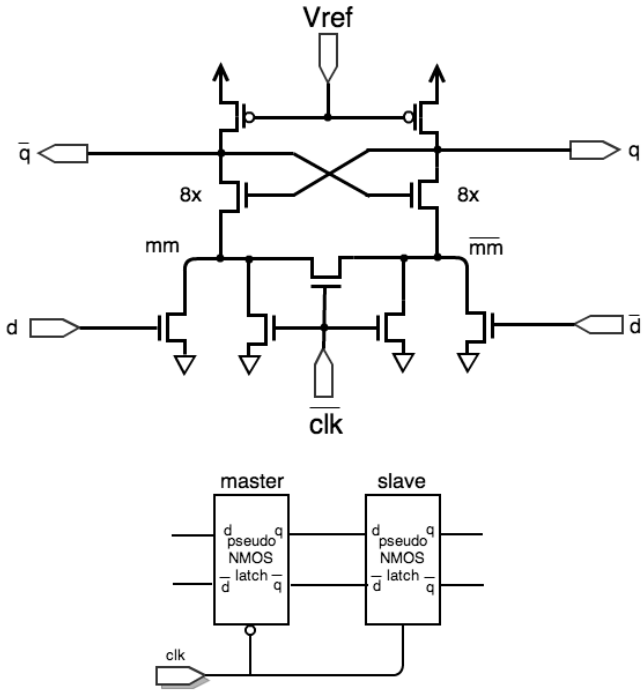
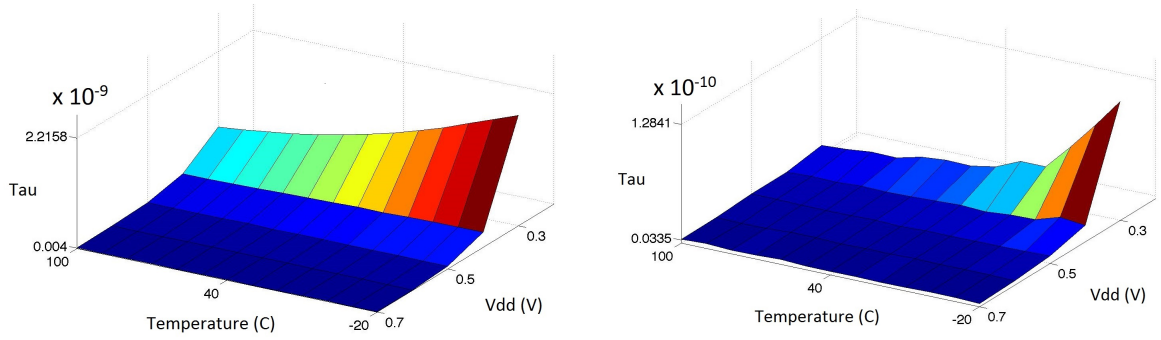
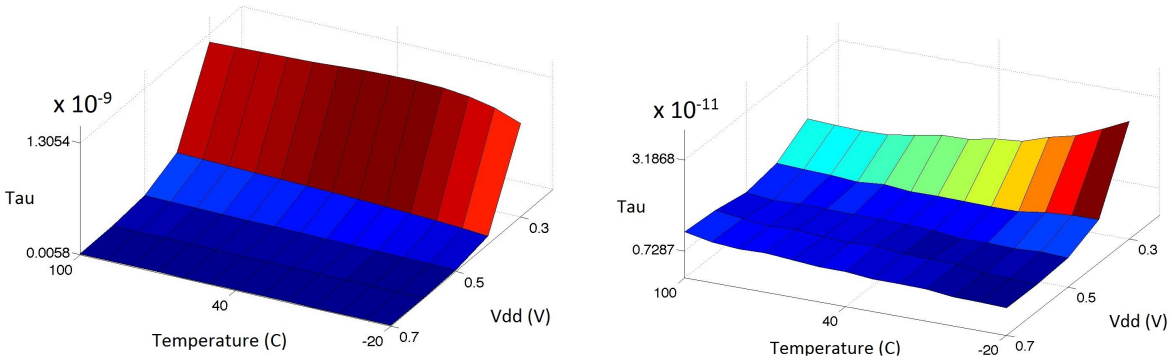


Fig. 5: Pseudo-NMOS Flip-Flop [2]



(a) 22nm Planar (b) 20nm FinFET

Fig. 6: DLFF τ with $Temperature$ and V_{DD} sweep



(a) 22nm Planar (b) 20nm FinFET

Fig. 7: Pseudo-NMOS τ with $Temperature$ and V_{DD} sweep

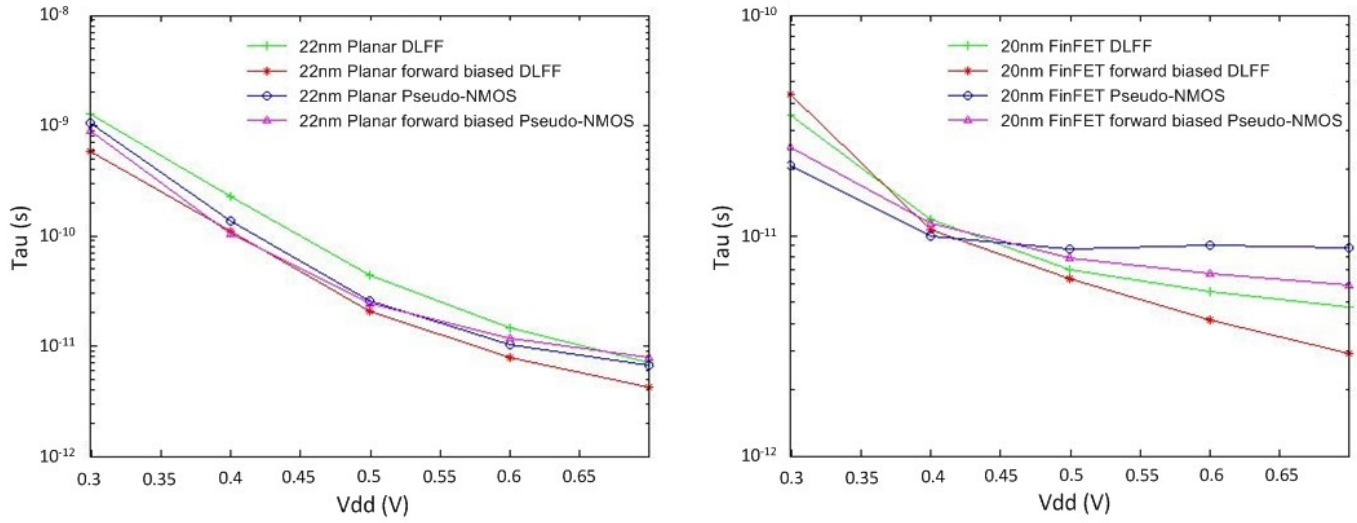
effect of FinFET devices has not yet been considered. Analysis from UC Berkeley has found that propagation delay in FinFET circuits is independent of electrical width [19]. This serves to maintain the gain of inverter built with FinFET devices, even as they are scaled. The factor of consideration relating τ and $FO4$ delay is inverter gain, and so it stands to reason that τ will continue to track $FO4$ delay even when using FinFETs.

This analysis is validated by the simulation results shown in Fig.2. Each of the three synchronizer flip-flops were simulated with a nominal V_{DD} of 0.7V and temperature of 22°C. The expected range for τ delay is between 0.2 and 1.5 times the given technology node's FO4 delay [4], and each of the three flip-flops tested fall within this range. While there is some variation between technology nodes, the results still match physically measured results by other researchers for planar technology nodes [2]. The FinFET nodes (7nm, 10nm, and 20nm) stay within the same $\frac{\tau}{FO4}$ range as the values found for planar nodes (22nm, 50nm).

B. τ and Temperature

As the temperature of a CMOS circuit increases, the carrier mobility is reduced (due to an increase in particle scattering) and the threshold voltage decreases. While these effects have opposite effects on CMOS speed, the decrease in mobility is more dominant for most circuits (higher temperatures mean slower logic) [20]. However, previous work has verified that the threshold voltage's temperature sensitivity is more important than mobility's sensitivity for synchronizer circuits, resulting in an increase in synchronizer τ with lower temperatures [7], [21]. FinFET devices are not affected by temperature in the same way as planar devices however. Recent work has found that the previously weaker voltage threshold effect is actually dominant in FinFET logic gates, which has led to an increase in logic gate performance at higher temperatures [22]. Unfortunately, this suggests a sharp increase in τ at lower temperatures for synchronizers built with FinFET devices.

The simulation results, shown in Fig. 6 and Fig. 7, do validate the theory predicting significantly higher τ values for FinFETs at low temperatures. While simulation was completed for all nodes mentioned before, 22nm planar and 20nm FinFET are shown here due to their similar physical dimensions. There is a more stark degredation (increase) of synchronizer τ at lower temperatures for circuits built with FinFET devices (7nm and 20nm). When built with planar devices in 22nm and 50nm technology, the DLFF and Pseudo-NMOS flip-flop are generally stable over temperature, even with low supply voltages. Therefore a general increase in temperature dependence with scaling can also be observed. The PowerPC flip-flop experienced these same effects, but its associated data is not displayed here in order to conserve space.



(a) 22nm Planar

(b) 20nm FinFET

Fig. 8: DLFF and Pseudo-NMOS τ when Non-Biased or Forward-Biased with V_{DD} sweep

These results also show that increases in τ due to lower temperatures can be prevented with a higher supply voltage. This further demonstrates that the dominant factor in synchronizer dependence on temperature is the change in threshold voltage. In modern SoCs, maximum restrictions on the supply voltage are generally enforced to prevent an increase in power consumption which leads to heat. Fortunately, this means that raising the supply voltage in a low temperature state to prevent τ degradation is not unreasonable.

C. Forward Biasing

Designers must also consider how FinFET devices will affect the trade-offs between various synchronizing flip-flop types. When all circuits were implemented with FinFET devices, the Power-PC flip-flop continued to be out-performed by both the DLFF and Pseudo-NMOS. However, the choice between the DLFF and Pseudo-NMOS becomes more complex when FinFET devices are used.

The DLFF was one of the first synchronizing flip-flops to be proposed, and relies on inverter feedback loops to settle metastability [9]. When near-threshold operation became more common, it was shown that inverter loops provided very poor τ at low voltages. For this reason, the Pseudo-NMOS flip-flop was proposed as a synchronizing flip-flop without the need for an inverter feedback loop [2]. Around the same time, another solution was proposed. This solution applied forward body bias to increase DLFF performance at low voltages [8]. It was demonstrated that forward body biasing increases the transconductance of the bi-stable inverter pair, resulting in a decrease in τ. While the Pseudo-NMOS has been compared to the unbiased DLFF, it has not yet been compared when using this technique. It is important to determine which design outperforms the other at low voltages, as well as verification of the technique's effectiveness when using FinFET devices.

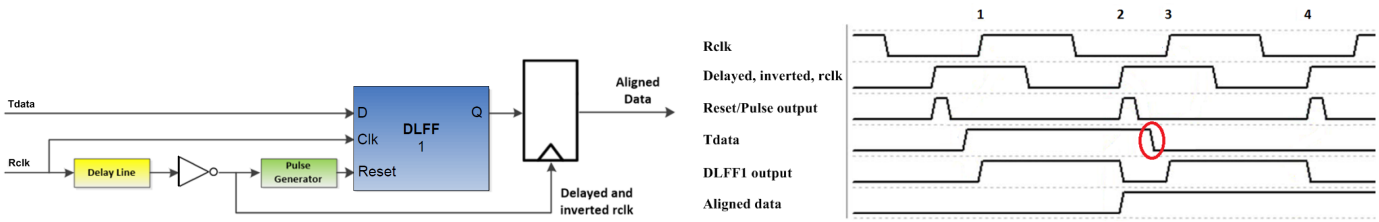
For 22nm planar technology, Fig.8(a) shows that the non-biased DLFF has the worst τ. However, when forward body biasing is applied the DLFF τ is significantly decreased. It even surpasses the biased Pseudo-NMOS flip-flop, which is relatively unchanged. This demonstrates that forward biasing a planar DLFF is the best solution for both high and near-threshold voltage operation.

In FinFET technology, not only are all τ values significantly reduced (observe the scale in Fig.8(b) vs Fig.8(a)), the tradeoffs change. Since FinFET devices sit on top of the bulk, rather than being deposited inside the bulk (as in planar technologies), the effect changes. As can be seen in Fig.8(b), both the DLFF and Pseudo-NMOS receive an increase in τ rather than a decrease in τ when forward biasing is applied at low voltages. This effectively removes biasing as a suitable technique for near threshold operation.

It can also be seen however that DLFF maintains a significant advantage over the Pseudo-NMOS at higher supply voltages, and can still be improved with forward body biasing. This presents a switching point (around 0.43V for 20nm) when above that voltage the DLFF is superior, and below that voltage the Pseudo-NMOS is superior. This is because inverter feedback loops offer a significant advantage at higher voltages. If the supply voltage must decrease, this advantage wears off and the Pseudo-NMOS achieves the lowest τ for near threshold operation.

V. The Dynamic Synchronizer

Comparing the raw τ values of synchronizer flip-flops is important, but not the whole story. There are some limitations when these designs are used in real SoCs. While this work has found the DLFF to outperform the PowerPC and Pseudo-NMOS flip-flops when operated with a higher supply voltage, it requires a separate reset signal. Modern SoCs do not use reset, and so the use of this flip-flop has been limited. This



(a) Schematic (b) Timing Diagram

Fig. 9: Simple Dynamic Synchronizer

paper presents a new circuit which automatically generates the required reset signal: The Dynamic Synchronizer.

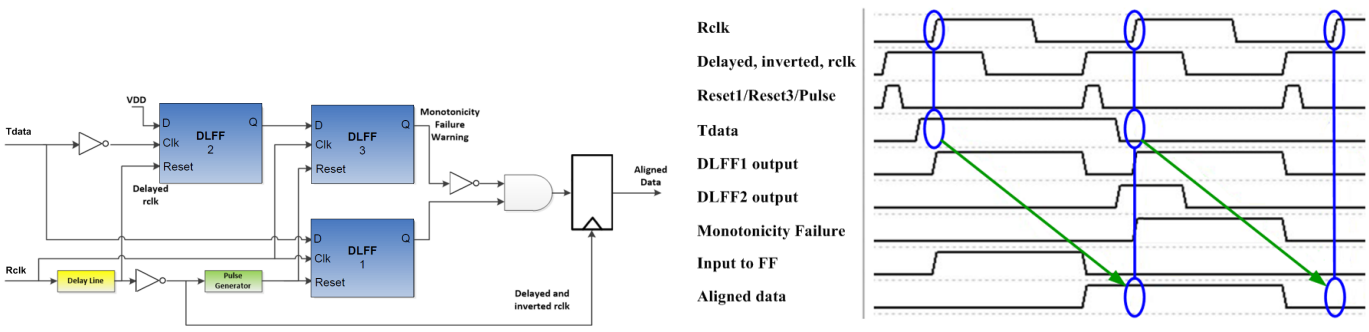
A simple version of the Dynamic Synchronizer is shown in Fig. 9(a), consisting of a single DLFF to sample data and resolve metastability. A normal D flip-flop is used to sample the output of the DLFF so that the output of the system is no longer affected by the periodic resets experienced by the DLFF. The output of this flip-flop is updated three-quarters of the way through the clock cycle.

The behavior of this circuit is described in more detail in Fig. 9(b). In timing event 1, a rising edge on *Rclk* causes DLFF1 to correctly sample a high value. Then, three-quarters of the way through the clock cycle, a rising edge on the *Delayed, inverted, rclk*, causes both the *Reset* of the DLFF1 (via a pulse shown in event 2) and the D flip-flop to sample the output of the DLFF1. While resetting and sampling the output of a DLFF at the same time might seem like it violates timing conditions, this is not the case and has been verified in both schematic and layout level simulations. This is similar to how each flip-flop in a brute-force synchronizer samples the flip-flop ahead of it, which is also sampling at that same time [23]. The data on the D flip-flop is now aligned and can be sampled by the receive clock domain on the next rising edge of *Rclk*.

Although the support structure around the DLFF has nearly hidden the dynamic behavior of this synchronizer, there is still one more eccentricity in the circuit's behavior. For one specific input combination, the Simple Dynamic Synchronizer will not sample the input properly. The situation in question is when *Tdata* experiences a falling edge in-between the falling edge of *Reset* and rising edge of *Rclk*. The circuit fails in this case because this input combination violates the monotonicity input restriction required of all dynamic circuits. The Simple Dynamic Synchronizer needs the *Reset* signal on the first flip-flop to pull its output down. If *Reset* is not asserted while the data experiences a falling edge, the synchronizer will keep sampling a high value until the reset can be reasserted.

The goal is to use this synchronizer in non-dynamic systems which do not maintain monotonic signals, so monotonic input cannot be assumed. In the case shown in Fig. 9(b) circled in red, *Tdata* experiences a falling edge in-between the falling edge of *Reset* and rising edge of *Rclk*. This is the specific situation which causes a problem. Since the DLFF circuit has no pull up transistors on its data input (see Fig. 3), the output of the inverter pair can only be truly pulled low with a *Reset* signal. In this case the falling edge on the data occurred after the reset, so the latches inside the DLFF remained in their high state. This can be observed at timing event 3, where the *DLFF1 output* incorrectly samples a logic high. This is then sampled by the conventional flip-flop, and the *Aligned data* incorrectly displays another high value. The output of DLFF1 is finally pulled low when the next *Reset* pulse occurs (timing event 4), and on the next rising edge of the *Rclk* the real data value will be seen.

This problem can be solved with a more robust design shown in Fig. 10(a). Since the problem is caused by a falling edge on *Tdata* between the falling edge of the *Reset* and the rising edge of *Rclk*, it is known that the false value caused will always be a false high value. For this reason, an AND gate has been inserted in between DLFF1 and the conventional flip-flop. This gates the output of DLFF1 and allows for a detection



(a) Schematic (b) Timing Diagram

Fig. 10: Robust Dynamic Synchronizer

circuit to force the output low when it detects a failure.

The detection circuit consists of two DLFFs, labeled DLFF2 and DLFF3 as shown in Fig. 10(a). The data input of DLFF2 is connected directly to V_{DD} while its clock input is connected to inverted *Tdata*. This means that a falling edge on *Tdata* will cause DLFF2 to always sample a high value. So that DLFF2 is only active during the period of interest, its Reset is connected to *Delayed rclock*. This means that DLFF2 is only active in-between the falling edge of *Delayed rclock* and when DLFF3 samples the output of DLFF2 with the rising edge of *Rclk*. The output of DLFF2 will only be high when *Tdata* experiences a falling edge (causing a rising edge on the DLFF2 clk input), causing V_{DD} to be sampled. This is then transferred over to DLFF3 on every rising edge of *Rclk* for evaluation. If the output of DLFF3 (*Monotonicity Failure*) is high, that means that there has been a monotonicity failure, and so this signal forces the output of the AND gate low. This supplies the conventional flip-flop with the correct data. So when the rising edge of the *Delayed, inverted, rclk* occurs, the conventional flip-flop supplies the correct *Aligned data* even though there was a monotonicity violation. DLFFs are used purposefully in the detection circuit, since metastability could occur if Reset was released at the same time as a falling edge of Tdata. The behavior of the Dynamic Synchronizer can be seen in Fig. 10(b). With the new *Monotonicity Failure* signal, the output of the DLFF1 can be corrected. The green arrows show the sampled values at each *Rclk* appearing correctly, ready to be sampled from *Aligned data* one cycle later.

While using DLFFs decreases the chance for metastability to be found on the output of the synchronizer, it does not eliminate that chance. For this reason, longer periods to settle metastability may be beneficial. The time period given to settle metastability is shown as S in the Equation (1). To accomplish this increase in S, additional stages can be added to add extra clock cycles of latency.

VI. Conclusions

The work in this paper has demonstrated and evaluated the changes expected as synchronizers begin to be designed exclusively with FinFET devices. First, results have been presented which demonstrate a continuing relationship between τ and $FO4$ delay as technology scales. This includes synchronizers built with both planar and FinFET devices. Forward body biasing has proven to still be effective in reducing τ, but its benefit has decreased. FinFET devices have also been shown to exacerbate τ degradation at low temperatures. Recommendations have been made to increase the supply voltage during periods of low temperature operation.

A comparison between high performance synchronizer flip-flop designs has also been presented. The DLFF has demonstrated lower τ at standard supply voltages, and the Pseudo-NMOS flip-flop has lower τ at lower supply voltages. Previously a separate reset signal was needed to use the DLFF, but the new synchronizer circuit presented here solves this problem. The Dynamic Synchronizer uses a locally generated reset and monotonicity detector to leverage the speed of the DLFF while hiding dynamic behavior. This allows systems which employ NoCs to benefit from the high performance DLFF (while at standard voltages) without the need for a separate reset signal.

References

[1] T. J. Chaney and F. U. Rosenberger, "Characterization and scaling of mos flip flop performance in synchronizer applications," 1979.

[2] S. Yang, I. Jones, and M. Greenstreet, "Synchronizer performance in deep sub-micron technology," in *Asynchronous Circuits and Systems (ASYNC), 2011 17th IEEE International Symposium on*, 2011.

[3] M. Baghini and M. Desai, "Impact of technology scaling on metastability performance of CMOS synchronizing latches," in *Design Automation Conference*, 2002.

[4] S. Beer, R. Ginosar, M. Priel, R. Dobkin, and A. Kolodny, "The devolution of synchronizers," in *Asynchronous Circuits and Systems (ASYNC)*, 2010.

[5] R. D. S. Beer and R. Ginosar, "Metastability measurements of several ASIC and FPGA synchronizers," in *Technical Report, EE Dept, Technion, Oct*, 2009.

[6] S. Sinha, G. Yeric, V. Chandra, B. Cline, and Y. Cao, "Exploring sub-20nm finfet design with predictive technology models," in *Design Automation Conference (DAC)*, 2012.

[7] S. Beer, R. Ginosar, J. Cox, T. Chaney, and D. M. Zar, "Metastability challenges for 65nm and beyond; simulation and measurements," in *Design, Automation and Test in Europe Conference and Exhibition*, 2013.

[8] J. Zhou, M. Ashouei, D. Kinniment, J. Huisken, G. Russell, and A. Yakovlev, "Sub-threshold synchronizer," *Microelectronics Journal*, 2011.

[9] C. Dike and E. Burton, "Miller and noise effects in a synchronizing flip-flop," *Solid-State Circuits, IEEE Journal of*, 1999.

[10] S. Beer, J. Cox, T. Chaney, and D. Zar, "MTBF bounds for multistage synchronizers," in *Asynchronous Circuits and Systems (ASYNC)*, 2013.

[11] D. Li, P. I.-J. Chuang, D. Nairn, and M. Sachdev, "Design and analysis of metastable-hardened flip-flops in sub-threshold region," in *Proceedings of the 17th IEEE/ACM international symposium on Low-power electronics and design*. IEEE Press, 2011.

[12] J. Horstmann, H. Eichel, and R. Coates, "Metastability behavior of CMOS ASIC flip-flops in theory and test," *Solid-State Circuits, IEEE Journal of*, 1989.

[13] L. Portmann and T. H. Meng, "Metastability in CMOS library elements in reduced supply and technology scaled applications," *Solid-State Circuits, IEEE Journal of*, 1995.

[14] J. Zhou, D. Kinniment, C. Dike, G. Russell, and A. Yakovlev, "On-chip measurement of deep metastability in synchronizers," *Solid-State Circuits, IEEE Journal of*, 2008.

[15] D. Rennie, D. Li, M. Sachdev, B. Bhuva, S. Jagannathan, S. Wen, and R. Wong, "Performance, metastability and soft-error robustness tradeoffs for flip-flops in 40nm CMOS," in *Custom Integrated Circuits Conference (CICC), IEEE*, 2011.

[16] S. Beer, R. Ginosar, M. Priel, R. Dobkin, and A. Kolodny, "An on-chip metastability measurement circuit to characterize synchronization behavior in 65nm," in *Circuits and Systems (ISCAS)*, 2011.

[17] A. Bhoj and N. Jha, "Design of ultra-low-leakage logic gates and flip-flops in high-performance finfet technology," in *Quality Electronic Design (ISQED)*, 2011, pp. 1–8.

[18] H. Khan, D. Mamaluy, and D. Vasileska, "Simulation of the impact of process variation on the optimized 10-nm finfet," *Electron Devices, IEEE Transactions on*, vol. 55, no. 8, pp. 2134–2141, 2008.

[19] A. Sachid and C. Hu, "A little known benefit of FinFET over planar MOSFET in highperformance circuits at advanced technology nodes," in *SOI Conference (SOI)*, 2012.

[20] N. Weste and D. M. Harris, *CMOS VLSI Design, A Circuits and Systems Perspective, Fourth Edition*, M. Hirsch, Ed. Addison-Wesley, 2011.

[21] J. Zhou, D. Kinniment, G. Russell, and A. Yakovlev, "Adapting synchronizers to the effects of on chip variability," in *Asynchronous Circuits and Systems (ASYNC)*, 2008, pp. 39–47.

[22] S. Soleimani, A. Afzali-Kusha, and B. Forouzandeh, "Temperature dependence of propagation delay characteristic in FinFET circuits," in *Microelectronics (ICM)*, 2008.

[23] R. Ginosar, "Metastability and synchronizers: A tutorial," *Design Test of Computers, IEEE*, 2011.